

CLAIMS

1. (currently amended) A memory comprising:  
a plurality of memory cells;  
a write line for writing a data value in the plurality of cells.  
a transistor coupled to the write line for controlling current in the write line, the transistor  
having a control electrode; and  
a first switch circuit having a first terminal coupled to the control electrode of the  
transistor and a second terminal coupled to a reference voltage circuit for  
providing a reference voltage for controlling an amount of current flowing  
through the write line during a write operation of memory, wherein the first  
switch circuit has a conductive state responsive to at least one of a timing signal  
or an enable signal.
2. (currently amended) The memory of claim 1 wherein the conductive state of the first  
switch circuit is responsive to both the timing signal and the enable signal.
3. (original) The memory of claim 1 further comprising:  
a second switch circuit having a first terminal coupled to the control electrode and a  
second terminal coupled to a voltage source having a voltage level such that when  
the second switch circuit is in a conductive state, the transistor is non conductive,  
wherein the second switch circuit has a conductive state responsive to at least one  
of the timing signal or the enable signal.
4. (original) The memory of claim 3 wherein when the first switch circuit is conductive, the  
second switch circuit is non conductive, and wherein when the first switch circuit is non  
conductive the second switch circuit is conductive.
5. (original) The memory of claim 1 wherein:  
the reference voltage circuit includes a current source and a diode connected transistor  
coupled in series to the current source.

6. (original) The memory of claim 5 wherein the reference voltage circuit further comprises a buffer circuit coupled to the second terminal.
7. (original) The memory of claim 1 wherein the transistor includes a first current terminal connected to the write line and a second current terminal connected to a voltage source.
8. (original) The memory of claim 1 wherein when the transistor is enabled for conducting a write current, the transistor operates in a saturation mode.
9. (original) The memory of claim 1 wherein the write line provides current to the plurality of memory cells to create a magnetic field for writing a data value to the plurality of memory cells.
10. (original) The memory of claim 1 wherein the transistor has a first current electrode coupled to the write line and a second current electrode coupled to a voltage source, the memory further comprising:
  - a capacitor having a first electrode coupled to the second current electrode of the transistor and a second electrode coupled to the second terminal of the first switch circuit;
  - a second switch circuit coupled between the second terminal of the switch circuit and the voltage reference circuit, the second switch circuit has a conductive state responsive to at least one of the timing signal or the enable signal.
11. (original) The memory of claim 1 wherein the reference voltage circuit comprises:
  - a reference transistor having a source coupled to a first power supply terminal, a gate, and a drain;
  - a reference resistance having a first terminal coupled to a second power supply terminal, and a second terminal coupled to the drain of the reference transistor;
  - an amplifier have a first input for receiving a bias voltage, a second input coupled to the drain of the reference transistor, and an output coupled to the gate of the reference transistor, wherein the output provides the reference voltage.

12. (original) The memory of claim 11 further comprising:  
a current source having a first terminal coupled to the first power supply terminal, and a second terminal providing the bias voltage; and  
a resistor having a first terminal coupled to the second terminal of the current source and a second terminal coupled to the second power supply terminal
13. (currently amended) The memory of claim 1, further comprising:  
a second switch circuit having a first terminal coupled to the control electrode and a second terminal coupled to the reference voltage circuit such that when the second switch circuit is in a conductive state, the transistor is non conductive, wherein the second switch circuit has a conductive state responsive to at least one of the timing signal or the enable signal.
14. (currently amended) A memory comprising:  
a plurality of memory cells;  
a plurality of write lines, each write line for writing a data value to a group of memory cells of the plurality of memory cells;  
a plurality of transistors, each transistor of the plurality of transistors coupled to a write line of the plurality of write lines for controlling ~~the~~ a current of the write line;  
a plurality of switch circuits, each switch circuit having a first terminal coupled to a control electrode of a transistor of the plurality of transistors, each switch circuit including a second terminal coupled to a reference voltage circuit for providing a reference voltage for controlling an amount of the current flowing through a write line, wherein each switch circuit has a conductive state responsive to at least one of a timing signal or an enable signal of a plurality of enable signals.
15. (currently amended) The memory of claim 14 wherein:  
each enable signal of the plurality of enable signals is associated with a transistor of the plurality of transistors; and  
each switch circuit of the plurality of switch circuits has a conductive state responsive to at least the enable signal that is associated with the transistor of the plurality of

transistors that has a control electrode coupled to the first terminal of the switch circuit.

16. (original) The memory of claim 14 wherein each switch circuit of the plurality of switch circuits has a conductive state responsive to both the timing signal and the one of the plurality of enable signals.

17. (currently amended) The memory of claim 14 wherein:  
the plurality of memory cells is arranged in rows and columns;  
each write line is for writing a data value to a column of memory cells of the plurality of memory cells;  
the memory further comprises:  
a second plurality of write lines, each write line of the second plurality for writing a data value to a row of memory cells of the plurality of memory cells;  
a second plurality of transistors, each transistor of the second plurality is coupled to a write line of the second plurality of write lines for controlling ~~the~~ a current of the write line;  
a second plurality of switch circuits, each switch circuit of the second plurality having a first terminal coupled to a control electrode of a transistor of the second plurality of transistors, each switch circuit of the second plurality has a second terminal coupled to a second reference voltage circuit for providing a reference voltage for controlling an amount of current flowing through a write line of the second plurality of write lines, wherein each switch circuit of the second plurality of switch circuits has a conductive state responsive to at least one of a second timing signal or an enable signal of a second plurality of enable signals.

18. (original) The memory of claim 17 wherein for each memory cell of the plurality, a write line of the first plurality and a write line of the second plurality each provide current to the memory cell to create a magnetic field for writing a data value to the memory cell.

19. (cancelled)

20. (original) The memory of claim 14 wherein each transistor of the plurality of transistors has a first current electrode coupled to the write line of the plurality of write lines and a second current electrode coupled to a voltage source, the memory further comprising:
- a plurality of capacitors, each capacitor having a first electrode coupled to the second current electrode of a transistor of the plurality of transistors and a second electrode coupled to a second terminal of a switch circuit of the plurality of switch circuits;
  - a plurality of second switch circuits, each switch circuit of the second plurality of switch circuits is coupled between a second terminal of a switch circuit of the plurality and the voltage reference circuit, each switch circuit of the second plurality has a conductive state responsive to at least one of a timing signal or an enable signal of the plurality of enable signals.
21. (original) The memory of claim 14 wherein:
- the reference voltage circuit includes a current source and a diode connected transistor coupled in series to the current source.
22. (original) The memory of claim 21 wherein for each transistor of the plurality of transistors, the reference voltage circuit acts as a first stage of a current mirror and the transistor acts as the second stage of a current mirror when a switch circuit of a plurality of switch circuits having a first terminal coupled to the control electrode of the transistor is in a conductive state.
23. (original) The memory of claim 21 wherein the reference voltage circuit further comprises a buffer circuit having an output coupled to the first terminal of each switch circuit of the plurality of switch circuits.
24. (original) The memory of claim 14 wherein each transistor of the plurality of transistors includes a first current terminal connected to a write line of the plurality and a second current terminal connected to a voltage source.
25. (original) The memory of claim 14 wherein for each transistor of the plurality, when the transistor is enabled for conducting a write current, the transistor operates in a saturation mode.

26. (original) The memory of claim 14 wherein the reference voltage circuit comprises:  
bias means for providing bias voltage representative of a desired voltage applied across  
the write lines;  
a reference transistor having a gate and a drain; and  
reference means, coupled to the transistor and the bias means, for providing the reference  
voltage by determining a gate voltage applied to the gate of the reference  
transistor that provides the desired voltage on the drain of the reference transistor.
27. (cancelled)
28. (original) A memory comprising:  
a plurality of memory cells;  
a write line for writing a data value in the plurality of cells.  
a transistor coupled to the write line for controlling current in the write line, the transistor  
having a control electrode;  
means for providing a control signal to the control electrode of the transistor, wherein  
when the control signal is not asserted, no current flows through the transistor,  
and when the control signal is asserted, the control signal has a voltage that  
controls an amount of current flowing through the transistor.
29. (original) The memory of claim 28 wherein the means is responsive to assert the control  
signal in response to at least one of a timing signal or an enable signal.
30. (original) The memory of claim 28 wherein the means is responsive to assert the control  
signal in response to both the timing signal and the enable signal.
31. (currently amended) The memory of claim 28 wherein the write line provides current to  
the plurality of memory cells to create a magnetic field for writing a data value to the plurality of  
memory cells.

32. (currently amended) A memory comprising:  
a plurality of memory cells;  
a plurality of write lines, each write line for writing a data value to a group of cells of the plurality of memory cells;  
a plurality of transistors, each transistor of the plurality of transistors coupled to a write line of the plurality for controlling ~~the~~ a current of the write line;  
for each transistor of the plurality of transistors, means for providing a control signal to the control electrode of the transistor, wherein when the control signal is not asserted, no current flows through the transistor, and when the control signal is asserted, the control signal has a voltage that controls an amount of current flowing through the transistor.
33. (original) The memory of claim 32 wherein for each transistor of the plurality of transistors, the means is responsive to assert the control signal in response to at least one of a timing signal or an enable signal of a plurality of enable signals.
34. (original) The memory of claim 32 wherein for each transistor of the plurality, the means is responsive to assert the control signal in response to both the timing signal and the enable signal of the plurality of enable signals.